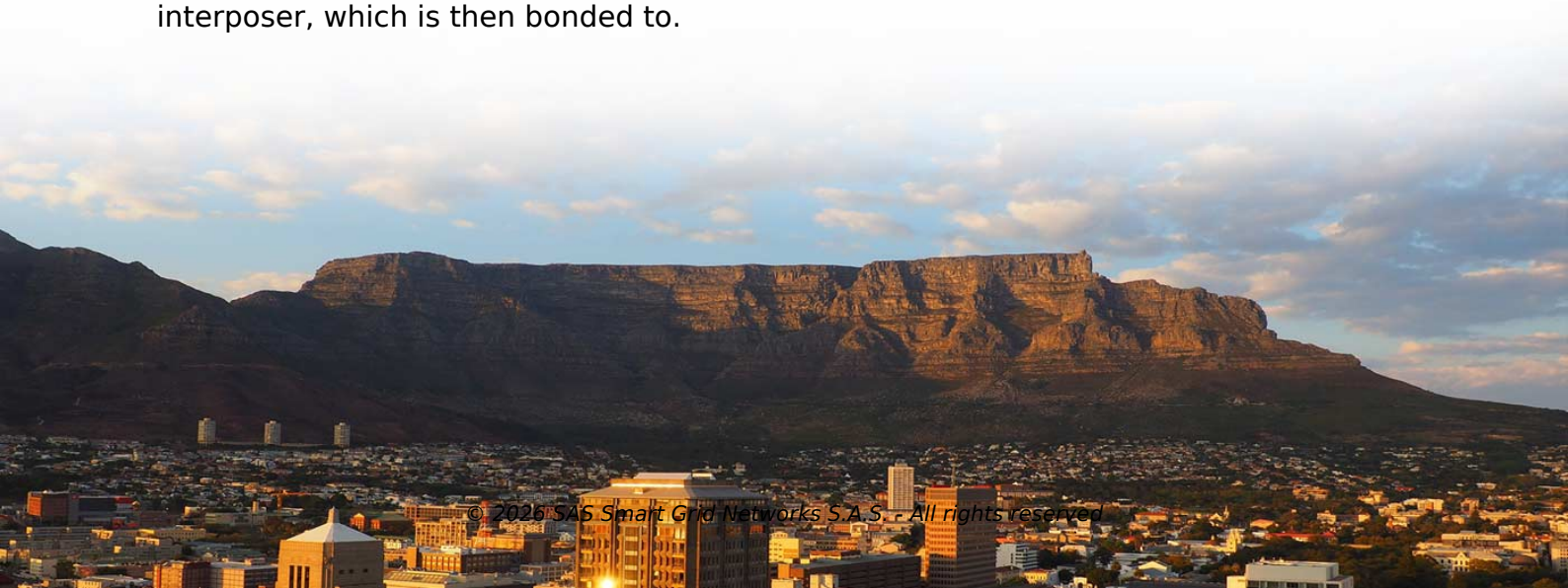
CoWoS-L Package and Optical Module

Overview

Full-wafer system integration with KGDs, compact size with integrated PWR supply and thermal modules. Low latency C2C communication and low PDN impedance. Higher BW density (2x): Superior line density due to fine pitch. TSMC's Chip on Wafer on Substrate with Silicon Interposer (CoWoS ® -S) provides best-in-class package technology for ultra-high performance computing applications, such as artificial intelligence (AI) and supercomputing. Wafer-level system integration provides high-density interconnects and deep. Chip-on-wafer-on-substrate (CoWoS) refers to the advanced packaging technology that offers the advantage of a larger package size and more I/O connections. 5D and 3D stacking of components to enable homogenous and heterogenous integration. Every NVIDIA H100, H200, B100, B200, GB200, and Rubin generation GPU ships on CoWoS. Y Hou (Director of Advanced Packaging Integration, gave a presentation on TSMC Advanced Co-packaged Optics (CPO) Integrated using Chip-on-Wafer-on-Substrate (CoWos) and Compact Universal Photonic Engine (COUPE) Readers of IFTLE are well. TSMC 's Chip-Scale Wafer-on-Size (CoWoS®) platform is a versatile 2. 5D packaging technology pioneered by TSMC. Unlike traditional SoC integration, CoWoS enables heterogeneous integration by combining multiple dies—such as SoCs, GPUs, and HBM memory stacks—on a silicon interposer, which is then bonded to.



Article Content

NVIDIA & Broadcom CPO, HBM4 & LPDDR6, TSMC Active LSI,

Optical Networking Several papers from major optics vendors tackled optical interconnects that will carry data between next-generation AI accelerators both within and between

What is TSMC COUPE and its role in photonics for AI

TSMC COUPE is a compact photonic engine integrated with SoIC-X that combines a 6nm EIC and a 65nm PIC, designed for very high speed and

Operational Highlights

New CoWoS®-L development targeting 5.5-reticle size interposer has been launched this year to meet higher performance goal in a package. In parallel, CoWoS® Co-packaged optics (CPO) for ultra-high

Status of High-End Performance Packaging (2.5D & 3D)

Enabling high-end performance applications with 2.5D / 3D packaging Intel, Samsung, and TSMC are leaders in the high-end performance packaging market space and key innovators in the field. With

Basket of 20 European stocks I like right now (and probably still will ...

Sole-source temporary bonders for CoWoS-L; capacity-constrained through 2027 against $TSM advanced packaging build-out. 12. $RPI (Raspberry Pi) - cos it tastes great.

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In a typical CoWoS package, TSMC usually combines multiple smaller dies and multiple HBM memory modules into a unified package that

NVIDIA Rubin GPU: 336B Transistors, T Orders

NVIDIA GTC 2026 unveiled Rubin with 336B transistors, 288GB HBM4, and 50 PFLOPS. Plus the 7B Nebius-Meta deal. Full architecture

The Packaging Fortress: TSMC''s $50 Billion Bet to Break the 2026 AI ...

TSMC''s massive $50 billion CapEx surge is a testament to the fact that the future of AI is being built in the packaging house, not just the foundry. With NVIDIA and AMD locked in a high

CPO & Silicon Photonics: AI''s Interconnect Bottleneck and Who Profits

2026 is the inflection point where co-packaged optics (CPO) moves from concept to volume production. The market routinely conflates two very different paths. One is ''optical

TSMC CoWoS and advanced CPO integration of COUPE technology

The successful integration of COUPE and CoWoS technologies in a single CPO package has brought the power efficiency and performance of high-performance computing and AI

TSMC 2026 Technology Symposium: Concrete, Steel, and Light

The most striking number was for CoWoS, the advanced packaging technology that stitches GPU dies to high-bandwidth memory in a single module.

Nvidia transitions to advanced CoWoS-L chip

Specifically, Nvidia is transitioning from CoWoS-S to CoWoS-L, representing a significant advancement in its chip architecture as well as a

Understanding CoWoS Packaging Technology

This section discusses the constituents of CoWoS-L package and the fabrication steps: CoWoS-L is a chip-last assembly because the interposer is fabricated

TSMC Our vision is to be the Business Overview most advanced and

rgeting 5.5-reticle size interposer has been launched this year to meet higher performance goal in a package. In parallel, CoWoS® Co-packaged optics (CPO) for ultra-high-end network switch is under

Celestial AI Photonic Fabric Module at Hot Chips 2025

Celestial AI Photonic Fabric Module Hot Chips 2025 CPO Differences Here is what this looks like with CoWoS-L with a chiplet that has the

Nvidia launches first US-made Blackwell chip with TSMC

Two US packaging sites are slated to start build in 2028 4 3. Their focus is System on Integrated Chips 3D stacking plus Co-Packaged Optics, not the CoWoS-L used by Blackwell 4 3.

Advanced Technology Leadership

Evolution of the SiPh package: from Pluggable Optics, On-Board Optics (OBO), to Co-Packaged Optics (CPO). High data rate and power efficiency could be achieved by monolithic integration. Technology

Inside Google''s Ironwood TPU v7 Supply Chain

It is a distributed profit pool spanning TSMC''s CoWoS capacity, SK hynix''s HBM ramps, ABF substrates, Celestica''s integration lines, and a long tail

TSMC CoPoS Packaging Technology: Next-Gen Panel-Level Solution

Phase 4 will be dedicated to large-scale CoPoS manufacturing. TSMC''s existing CoWoS production, meanwhile, will remain at its AP8 facility, formerly an Innolux plant. TSMC will initially

5.1 Business Activities

ance goal in a package. The further development of the 9.5-reticle size CoWoS®-L is al o making good progress. In parallel, CoWoS® Co-packaged optics (CPO) for ultra-high-end network switch is under

TSMC Boosts CoWoS Capacity as NVIDIA Dominates Advanced Packaging ...

TSMC''s CoWoS technology, specifically the CoWoS-L (Local Silicon Interconnect) variant, has become the gold standard for integrating multiple logic and memory dies. As of late

Complete Guide to CoWoS Process: The Key

Key to CoWoS-R and CoWoS-L variants, RDL enables flexible I/O routing and efficient use of substrate area. CoWoS-R uses organic substrates,

Chip on Wafer on Substrate (CoWoS) Guide

CoWoS®-L is one of the last for chip packages in the CoWoS® platform, combining the merits of CoWoS®-S and InFO technologies to provide the most flexible

TSMC''s CPO Integration: A New Era for High

By moving optics directly into the package, they are solving critical power and bandwidth challenges that threaten the progress of AI and HPC. For

TSMC''s annual Technology Symposium kicks off Wednesday (April

TSMC will detail its latest process and advanced packaging roadmaps: •A14 node with backside power delivery (BSPDN) and NanoFlex Pro technology — enabling wide + narrow

Top 10 Semiconductor Trends in 2026 | StartUs Insights

TSMC''s CoWoS-S interposers currently span ~3.3X reticle (~2700 mm2). This change is supported by NVIDIA''s packaging approach. Blackwell

IFTLE 642: TSMC Advanced Co-packaged Optics

TSMC is developing the integration of COUPE and CoWoS in one CPO package to bring the HPC/AI components to a new era in power and

CoWoS Advanced Packaging: Chip-on-Wafer-on-Substrate, TSMC

CoWoS-L is the growing variant for customers who need CoWoS-level integration without the full silicon-interposer cost, and it eases the pressure on CoWoS-S capacity by diverting customers who don''t

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